5. Circuit Description

5-1 Logic Section

5-1-1 Power Supply

With the battery installed on the phone and by pressing the END/ key, the VBATT and ON_SW signals will be connected. This will turn on U123 DC_DC convertor.
This in turn will be supplied to PIN3, PIN4 of regulators U124, PIN6 of regulators U122, thus releasing them from the shut-down state to output regulated 3.3V. (The VBATT applied to ON-SW will turn on Q103(DTC144EE) resalting in the signal ON-SW-SENSE to change start the from High to Low.)
The MSM recognizes this signal and sends out PS_HOLD (logical HIGH) to turn on Q102 even after the PWR key is released.
The power from U124 is used in the digital part of MSM and BBA. The power from U122 is used in analog part of BBA.

5-1-2 Logic Part

The logic part consists of internal CPU of MSM, RAM, ROM and EEPROM. The MSM receives TCXO and CHIPX8 clock signals from the BBA and controls the phone during the operation. The major components are as follows:

- CPU : INTEL 80186 core (inside the MSM)
- FLASH ROM : U129 - 8 Mbit FLASH MEMORY
- SRAM : U127 - 2 Mbit STATIC RAM
- FLASH ROM : U130 - 1 Mbit FLASH MEMORY
- EEPROM : U102 - 128 Kbit SERIAL EEPROM

CPU

INTEL 80186 CMOS type 16-bit microprocessor is used for the main processing. The CPU controls all the circuitry. For the CPU clock, 27MHz resonator is used.

FLASH ROM

One 8 MBIT FROM is used to store the terminal's program. Using the down-loading program, the program can be changed even after the terminal is fully assembled.

SRAM

One 2 MBIT SRAMs is used to store the internal flag information, call processing data, and timer data.

EEPROM

One 128 KBIT EEPROM is used to store ESN, NAM, power level, volume level, and telephone number.

KEYPAD

For key recognition, key matrix is setup using SCAN0-6 of STORE signals and KEY0-3 of input ports of MSM. Ten LEDs and backlight circuitry are included in the keypad for easy operation in the dark.

LCD MODULE

LCD module contains a controller which will display the information onto the LCD by 8-bit data from the MSM. It also consists a DC-DC converter to supply -3.5V for fine view angle and LCD reflector to improve the display efficiency.

5-1-3 Baseband Part

MOBILE SYSTEM MODEM (MSM)

The MSM equipped with the INTEL 80C186 CPU core is an important component of the CDMA cellular phone. The MSM comes in a 176 pins TQFP package.

MICROPROCESSOR INTERFACE

The interface circuitry consists of reset circuit, address bus (A0-A19), data bus (AD0-AD15), and memory controls (ALE, DT_R, HWR/, LWR/, RAM_CS/, ROM_CS).

INPUT CLOCK

- CPU clock: 27 MHz
- TXCO/4 (pin 34): 4.92 MHz. This clock signal from the BBA is the reference clock for the MSM except in CDMA mode.
- CHIPX8 : 9.8304 MHz. The reference clock used during the CDMA mode.

BBA INTERFACE

CDMA, FM Data Interface

- TXIQDATA0-7 (pins 24-32) : TX data bus used during both CDMA and FM mode but it is used only for CDMA mode at this phone.

Clock

- TC_CLK (pin 22), TX_CLK/(pin 23) : Analog to Digital Converter (ADC) reference clock used in TX mode.
- CHIPX8 : ADC reference clock used in CDMA RX mode.
- FMCLK: TXclock used in FM mode.

ADC Interface

ADC_CLK (pin 3), ADC_ENABLE (pin 1) and ADC_DATA (pin 2) are required to control the internal ADC in the BBA.

Data Port Interface

Includes the UART. Also, supports Diagnostic Monitor (DM), HP equipment interface, down loading, and data service.

CODEC Interface

The MSM outputs 2.048 MHz PCM_CLK (pin 19) and 8 KHz CODEC_SYNC (pin 16, 20) to the CODEC (U117). The voice PCM data from the MSM (U101) PCM_DIN (pin 135) is compressed into 8 KHz, by QCELP algorithm in the CDMA mode.

RF Interface

TX : TX_AGC_ADJ (pin 35) port is used to control the TX power level and PA_ON (pin 44) signal is used to control the power amplifier. This signal depends on the TX vocoder rate.

RX : AGC_REF (pin 36) port is used to control the RX gain and TRK_LO_ADJ (pin 45) is used to compensate the TCXO clock.

General Purpose I/O Register Pins

Input/output ports to control external devices.

Power Down Control

When the IDLE/ signal turns LOW, only the TX sections will be disabled. If both the IDLE/ and SLEEP/ change to LOW, all the pins except for the TCXO and 27MHz clock are disabled.

5-1-4 Audio Part

TX AUDIO PATH

The voice signal output from microphone is filtered and amplified by the internal OP-AMP and is converted to PCM data by the CODEC (U117). The signal is then applied to the MSM (U101)'s internal vocoder.

RX AUDIO PATH

The PCM data from the MSM's converted to audio signal by ADC of CODEC (U117), is then amplified by the speaker amplifer (U111) to be sent to the speaker unit.

TX WBD, ST,SAT

These signals are generated from MSM. The modulation level of TX WBD and ST is 8 kHz/dev, and SAT is ° 2 kHz/dev.

BUZZER DRIVING CIRCUITY

Buzzer generates alert tone when the buzzer receives the timer signal from the MSM, it generates alert tone. The buzzer level is adjusted by the alert signal's period generated from the MSM timer.

KEY TONE GENERATION

Ringer signal (pin49) out from MSM (U101) is passed through 2 serial LPF consisting of R141, C146, R145, and C142 amplified at the speaker amp (U111), and comes out to speaker.

5-2 Receiver Section

LOW NOISE AMPLIFIER (LNA, Q302)

The low noise amplifier amplifies a weak signal received from the base station to obtain the optimum scvel (Noise figure = 1.5 dB, Gain = 16 dB).

RADIO FREQUENCY BAND PASS FILTER (RF BPF)

The RF BPF accepts only a specific frequency (881 °æ 12.5 MHz) from the signal received from the base station. The band width is 25 MHz.

DOWN CONVERTER (MIXER, U302)

First local signal is applied to this down converter. The down converter transfers the signal amplified at the LNA into 85.38 MHz IF signal. 85.38 MHz IF signal is made by subtracting 881 °æ12.5 MHz RF signal from 966 °æ12.5 MHz first local signal.

AUTOMATIC GAIN CONTROLLER (AGC) AMP U303)

85.38 MHz IF signal is applied to IF AGC amp, the IF AGC output level is applied to BBA (Baseband Analog ASIC). The IF AGC amp (U302) keeps the signal at a constant level by controlling the gain. Dynamic range is 90dB, up gain +45dB, and down gain -45dB.

IF BAND PASS FILTER (FOR CDMA)

IF SAW BPF (F303) is used for CDMA system having 1.23 MHz wideband and °æ630 kHz bandwidth. The filter also attenuates the image product generated at the mixer.

BUFFER AMP (Q385)

Buffer (Q385) amplifiers signal to be applied to the local input of the down converter (U301) when a phase is locked between VCO (U341) and PLL IC (U342).

VOLTAGE CONTROLLED OSCILLATOR (VCO, U341)

The VCO (U341) generates the signal having 966 MHz center frequency and °æ12.5 MHz deviation with the voltage control. PLL IC (U342) controls this signal.

ANTENNA

Antenna allows signals and send to receive from the base station.

PHASE LOCKED LOOP (PLL, U342)

Input reference frequency is generated at VC_TCXO (U343) and the divided signal is generated at VCO. PLL compares the two signals and generates the desired signal with a pre-programmed counter which controls voltage.

VOLTAGE CONTROLLED TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (VC-TCXO, U343)

It provides 19.68 MHz reference frequency to PLL. A correct frequency tuning is made by the voltage control.

DUPLEXER (F301)

Duplexer (F301) controls to transmit through the antenna only the signals within acceptable Tx frequency range (836 °æ12.5 MHz) and to receive through the antenna only the signals within acceptable Rx frequency range (881 °æ12.5 MHz). It also matches LNA input in receiving part and PA output in transmitter part with the antenna.

POWER SUPPLY REGULATOR (U382)

The power supply regulator generates a regulated power.

THERMISTOR (R498)

The thermistor (R498) detects temperature. It is used to compensate active component characteristics due to the temperature difference.

5-3 Transmitter Section

BBA (U401)

BBA (U401) consists of ADC, DAC, LPF (FM / CDMA), divider, VCO, logic control circuit, PLL, and mixer.

BBA performs a specific function between RF part and logic part, with MSM. The IF signal out from Rx IF AGC amp is secondly converted throuth the down-converter. The signal passes through the CDMA or FM filter, converts to digital signal through ADC, then is sent to MSM. The digital signal out from MSM converts to analog signal through each filter and the up-converters.

POWER AMP MODULE (U467)

Power Amp module (U467) amplifies signal (24dB Gain) to be sent out to the base station through the antenna.

UP CONVERTER (MIXER, U460)

The up-converter (U460) receives the first local signal to generate 836 °æ12.5 MHz from the BBA. 836 °æ12.5 MHz signal comes out of the mixer output by subtracting 130 MHz IF signal from 966 °æ12.5 MHz first local signal.

RF AUTOMATIC GAIN CONTROLLER AMP (U461, U464)

The signal out to the base station should be a constant level. The TX RF AGC amp controls power to keep the signal at a constant level.

RF BAND PASS FILTER (BPF, F451)

The RF BPF (F451) accepts only a specific frequency (836 °æ12.5MHz) to send it out to the base station. The band width is 25 MHz.

POWER SUPPLY SWITCHING (U484)

Power supply switching (Q484) turns on TX_POWER when the phone is in traffic mode and supplies power to the circuits.

POWER SUPPLY REGULATOR (U482, U483)

The power supply regulators (U482,U483) supply a regulated power to each part of transmitter. U482 supplies 3.6V to TX AGC amp (U461) and up-converter (U460). U483 supplies 3.0V to power amp module control circuit (U487).

5-4 Desk-Top Rapid Charger

The Desk-top rapid charger(DTC21) is largely divided by two parts. One part generates secondary static voltage and current from AC power source, and the other part detects the battery pack, the battery type, and charge voltage, and controls the charging status.

5-4-1 Power Supply

AC POWER PROTECTOR AND REGULATOR

The AC power is regulated through BD1, C2 and converted to the high DC voltage.

TNR1 is used for surge protector, F1 is fuse to protect from overcurrent, and C1 and LF1 are filters to eliminate the noise of the switching circuit.

SWITCHING CONTROLLER AND TRANSFORMER

U1 as a switching controller supplies static voltage and current to the secondary through U2 (photo coupler).

Transformer PTF1 is combined with the 4 winding coils. The primary winding is linked to the primary side and the secondary winding is linked to the secondary side so that it supplies power. The fourth winding is used to supply power to U1.

This SMPS circuitry uses a flyback method, so the secondary1, 2 and fourth coils are wound reversely against the primary. When the power applies to the primary, the secondary and third will be off. When the primary is power off, the saved power will apply to the secondary and U1.

D1, D2 is a snubber circuitry, and absorbs the counter-voltage which comes out when the primary winding is off.

STATIC ELECTRICAL CURRENT CIRCUITRY

The electric current which flows on the secondary winding is detected by R25. The current will be converted into proportional voltage through U23-A and Q21.

The proportional constant is changed according to the ON / OFF status of Q22, Q23, and Q24, so that it finally change the value of the static electrical current.

The Vi is added to the U24-A pin 2, and the voltage is compared with the reference voltage (Vr) of pin 3. When the Vi is greater than the Vr, Q36 turns on and the IC2-2 is activated.

At this time, IC2-1 becomes on. It makes IC1 be off, as a result, the primary will be off and limit the electric current output.

Assumes the static current on the secondary is lc, the Vi will be obtained by following below.

$$V = \frac{(R25 // R77)}{(R23 // R24)} Ic\ [R26 // (\bullet R27) // (\bullet , R28) // (\bullet „ R29)]$$

STANDARD : • ⊂° ƒ	EXTENDED : • ⊂° ƒ
• ,= 1	• ,=° ƒ
• „= ° ƒ	• „= 1

The Vi is maintained as the same level as Vr of the comparator U24-B, so Vi is Vr. That is:

$$IC = \frac{(R23 // R24)\ °§\ Vr}{(R25 // R77)\ [\ R26 // (\bullet R27) //\ (\bullet , R28) // (\bullet „ R29)]}$$

$$Vr = \frac{R48}{R47 + R48}\ Vcc$$

R68 and C49 are used to compensate the phase difference occured due to the time delay for the circuit.

STATIC VOLTAGE CIRCUIT (4.1V OUTPUT)

The secondary (cathod of D23) output voltage Vo is separated by R50, VR1, R55, R79 and applied to the comparator U24-B pin 6. Q41 turns off (10k~33k) or on (0~5.1k) according to the resistance value in V/F (front/rear) terminal of R50,R79.

In accordance, when Q41 turns on, the parallel linked resistance value of R50 and R79 become smaller, so that 4.1V comes out. The voltage will be compared with the reference input voltage of pin 5, and feedback to the primary by U2(OPT).

U24-B output voltage is linked to U24-A output. It turns Q36 off. Consequently, if either one of these static voltage or static current overflows, it will automatically turn U1 off. R45 and C36 are used to compensate the phase difference caused by the time delay.

$$Vd = \frac{R55}{(R50 // R79 + VR21) + R55} Vo$$

Since, the Vd is maintained to be the same level as the reference voltage Vr is,

$$Vo = \frac{(R50 // R79 + VR21) + R55}{R55} Vr$$

STATIC VOLTAGE CIRCUIT (4.2V OUTPUT)

The secondary (cathod of D23) output voltage Vo is separated by R50, VR21, R55, R79 and applied to the comparator U24-B pin 6. Q41 turns off (10k~33k) or on (0~5.1k) according to the resistance value in V/F (front/rear) terminal of R50, R79.

In accordance, when Q41 turns off, only the parallel linked resistance value of R50 is selected, so that 4.2V comes out. The voltage will be compared with the reference input voltage of pin 5, and feedback to the primary by U2.

U24-B output voltage is linked to U24-A output. It turns Q36 off. Consequently, if either one of these static voltage or static current overflows, it will automatically turn U2 off. R45 and C36 are used to compensate the phase difference caused by the time delay.

$$Vd = \frac{R55}{(R50 + VR21) + R55} Vo$$

Since the Vd is maintained to be the same level as the reference voltage Vr is,

$$Vo = \frac{(R50 + VR21) + R55}{R55} Vr$$

CHARGE SWITCHING CIRCUITRY

The rapid charger has two charge ports; front port and rear port.

When the battery is charged in the front port, Q35 turns on. It turns Q34-A (P-CHANNEL FET) on.

When the battery is charged in the rear port, Q33 turns on. It turns Q34-B (P-CHANNEL FET) on.

When the battery level becomes low, this circuitry will charge the battery until it reaches 2.7V with Q26 and Q39.

5-4-2 Controller

MICRO-CONTROLLER

U21 is a 4-bit micro-controller which controls the whole charging system. It contains I/O port, timer, and A/D converter. 4 MHz clock is used for the controller.

DETECTION OF CHARGE VOLTAGE

The battery voltage in the front port is detected by R60 and R61, and measured at the pin 13 of the MPU.

The battery voltage in the rear port is detected by R58 and R59, and measured at the pin 14 of the MPU through the analog switch U25. measured at the pin 14 of the MPU through U25.

DETECTION OF BATTERY TYPE

The battery type in the front port is detected by R54, R56, and the resistor which is connected between the battery C/F and ground terminal, and measured at the pin 15 of the MPU through U26.

The battery type in the rear port is detected by R53, R57, and the resistor which is connected between the battery C/F and ground terminal, and measured at the pin 15 of the MPU through U26.

DETECTION OF AMBIENT TEMPERATURE

TH21 is a thermistor which is used to detect the ambient temperature. It has a linear characteristic by R51 and R52, and is measured at the pin 14 of the MPU through U25.

MEASURING CHARGING CURRENT

The charging current is converted through U23-A to the voltage Vi which is proportional to the current. The noise of Vi is eliminated with R71 and C30. Finally the voltage Vi is measured at the pin 12 of the MPU.

AUTONOMOUS TIMER

If the MPU stops its operation with the charging port on due to an accidental shock (for example, drop), the battery may become overcharged. The external timer U23-B is equipped to protect the battery from being overcharged. If the timer is not reset within a specified time by MPU, MPU will be automatically reset by the timer.

MEMO